

$l$  is a completely fresh label.

## Loading and storing

Loading shared data

$$\frac{R(r_s) = l \quad H(l) = \langle \nu_0, \dots, \nu_n, \dots, \rangle}{(H, R, r_d := \text{Mem}[r_s + n]; I) \rightarrow (H, R \oplus \{r_d \mapsto \nu_n\}, I)} \quad (\text{E-Ld-S})$$

## Loading and storing

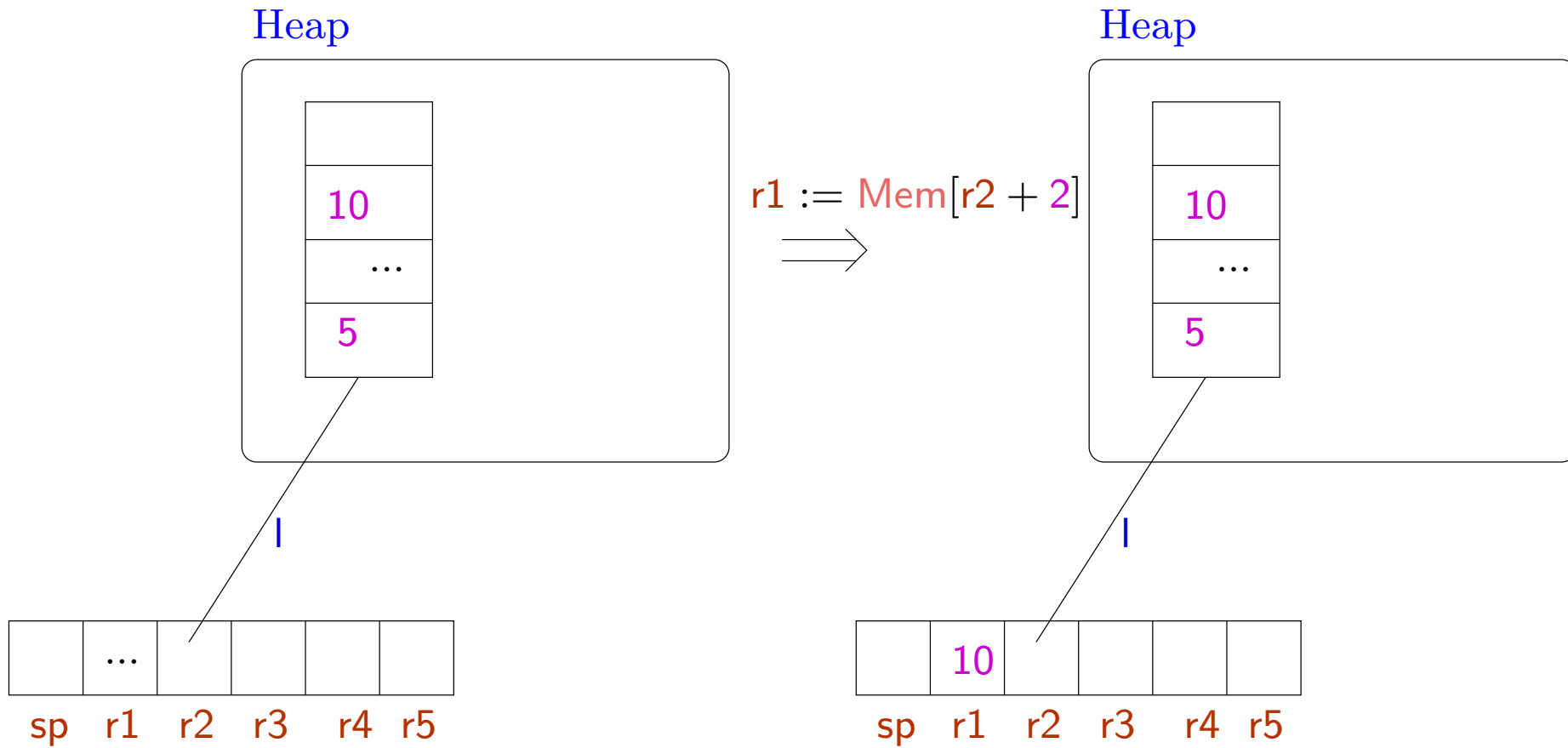
### Loading shared data

$$\frac{R(r_s) = l \quad H(l) = \langle \nu_0, \dots, \nu_n, \dots, \rangle}{(H, R, r_d := \text{Mem}[r_s + n]; I) \rightarrow (H, R \oplus \{r_d \mapsto \nu_n\}, I)} \quad (\text{E-Ld-S})$$

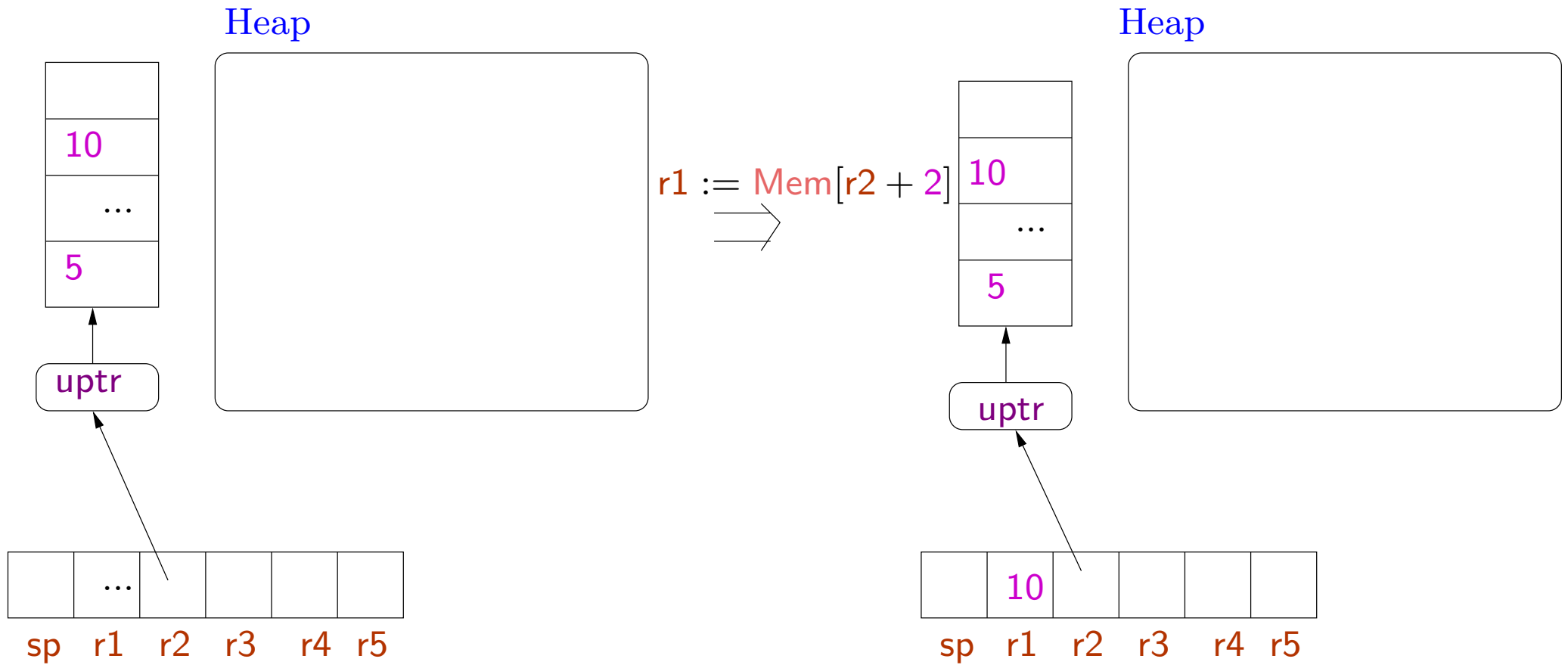
### Loading unique data

$$\frac{R(r_s) = \text{uptr} \langle \nu_0, \dots, \nu_n, \dots, \rangle}{(H, R, r_d := \text{Mem}[r_s + n]; I) \rightarrow (H, R \oplus \{r_d \mapsto \nu_n\}, I)} \quad (\text{E-Ld-U})$$

# Loading shared data



# Loading unique data



## Storing shared data

$$\frac{R(r_d) = l \quad H(l) = \langle \nu_0, \dots, \nu_n, \dots, \rangle \quad R(r_s) = \nu \quad \nu \neq \text{uptr}(h)}{(H, R, \text{Mem}[r_d + n] := r_s; I) \rightarrow (H \oplus \{l \mapsto \langle \nu_0, \dots, \nu, \dots, \rangle\}, R, I)} \quad (\text{E-St-S})$$

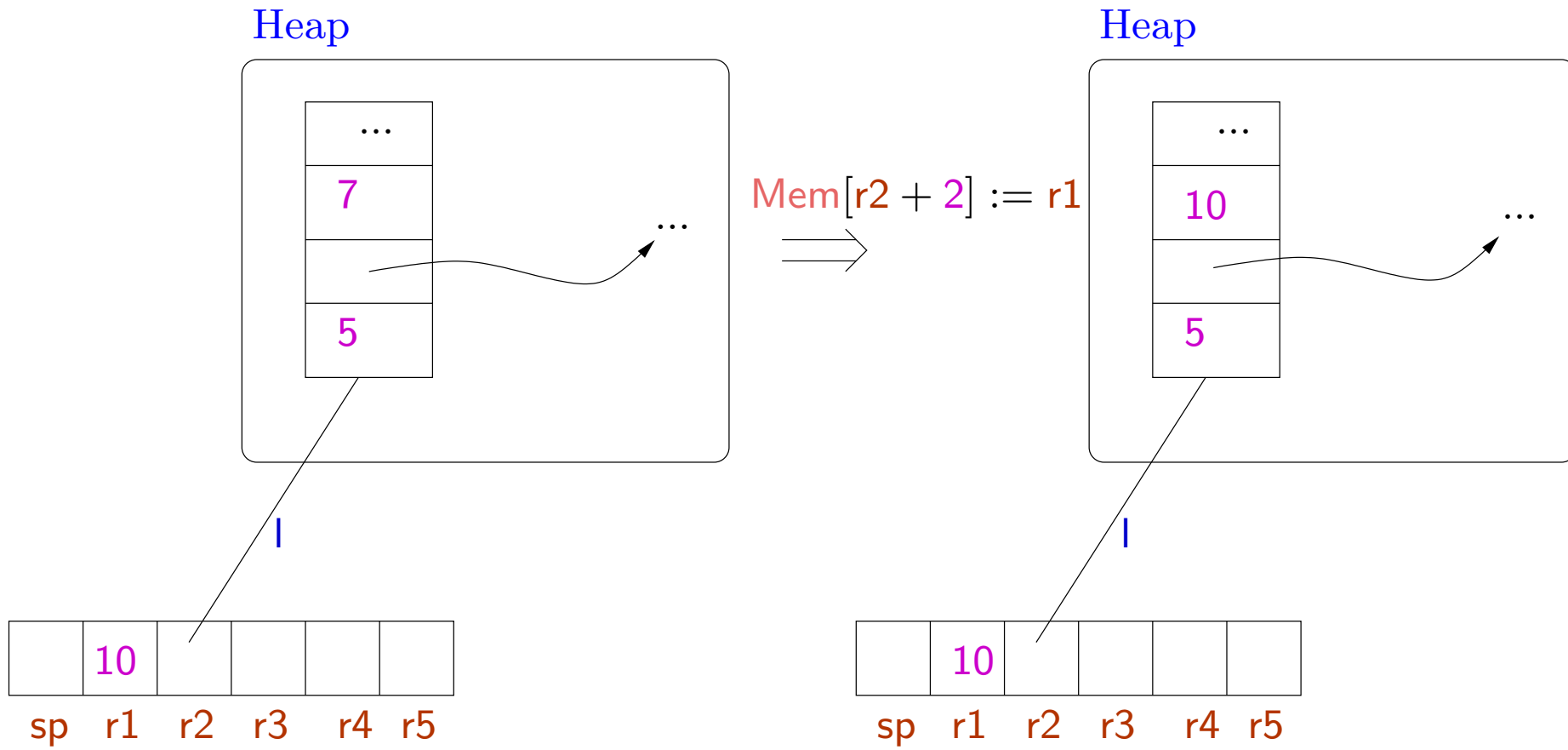
## Storing shared data

$$\frac{R(r_d) = l \quad H(l) = \langle \nu_0, \dots, \nu_n, \dots, \rangle \quad R(r_s) = \nu \quad \nu \neq \text{uptr}(h)}{(H, R, \text{Mem}[r_d + n] := r_s; I) \rightarrow (H \oplus \{l \mapsto \langle \nu_0, \dots, \nu, \dots, \rangle\}, R, I)} \quad (\text{E-St-S})$$

## Storing unique data

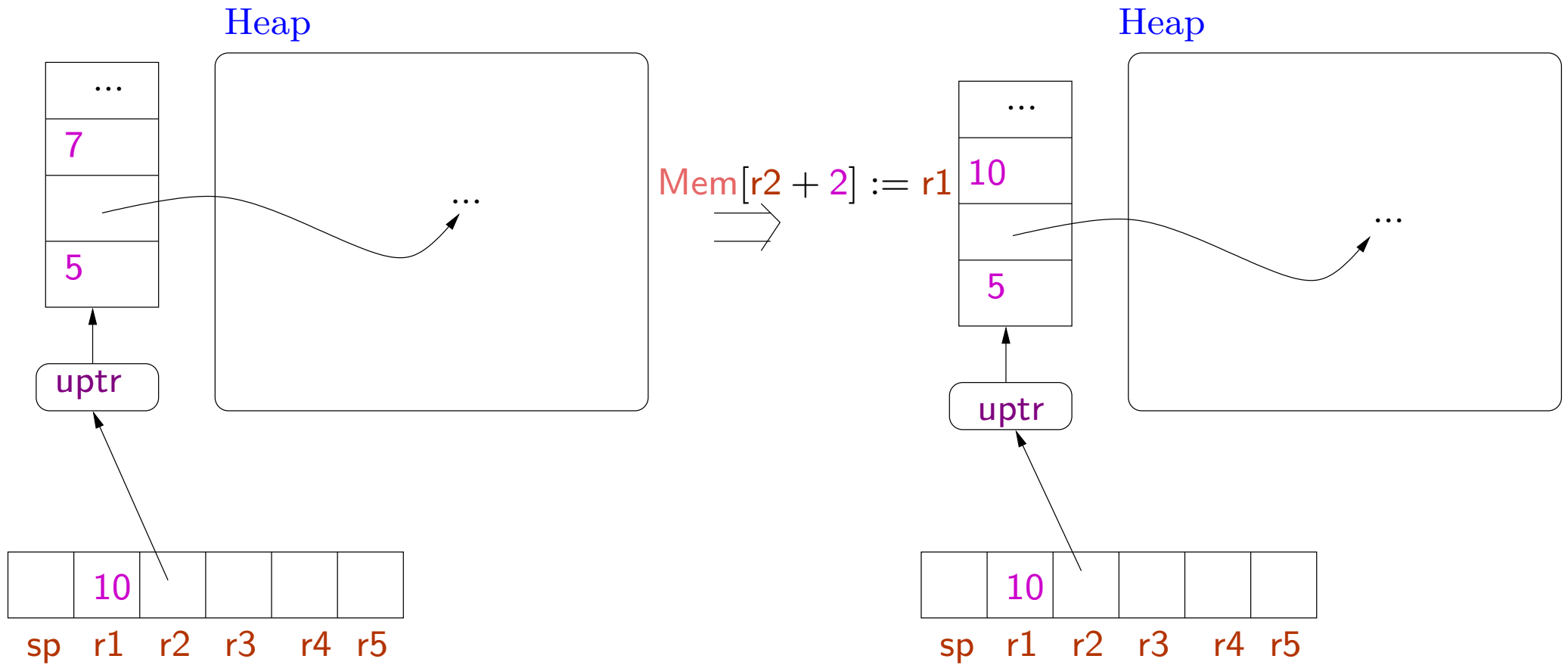
$$\frac{R(r_d) = \text{uptr}\langle \nu_0, \dots, \nu_n, \dots, \rangle \quad R(r_s) = \nu \quad \nu \neq \text{uptr}(h)}{(H, R, \text{Mem}[r_d + n] := r_s; I) \rightarrow (H, R \oplus \{r_d \mapsto \text{uptr}\langle \nu_0, \dots, \nu, \dots, \rangle\}, I)} \quad (\text{E-St-U})$$

# Storing shared data





# Storing unique data



Example Allocating space, initializing data, and making it shared.

```
l : r1 := malloc 3;
```

```
  r3 := l;
```

```
  r4 := 7;
```

```
  Mem[r1] = r3;
```

```
  Mem[r1 + 1] = r4;
```

```
  commit r1;
```

```
  r2 := r1;           // now the pointer can be aliased
```

```
  r4 := r4 + 6;
```

```
  Mem[r2 + 1] := r4; // this is ok (should be well-typed)
```

```
  Mem[r2 + 1] := r3; // this is not ok
```

This is also ok.

```
l : r1 := malloc 3;  
    r3 := l;  
    r4 := 7;  
    Mem[r1] = r4; //r1 : uptr(Int,...)  
    Mem[r1] = r3; //r1 : uptr(Code(...),...)  
    ...  
    commit r1;
```

Type of data can change before being declared to be shared.

## Allocation on the stack

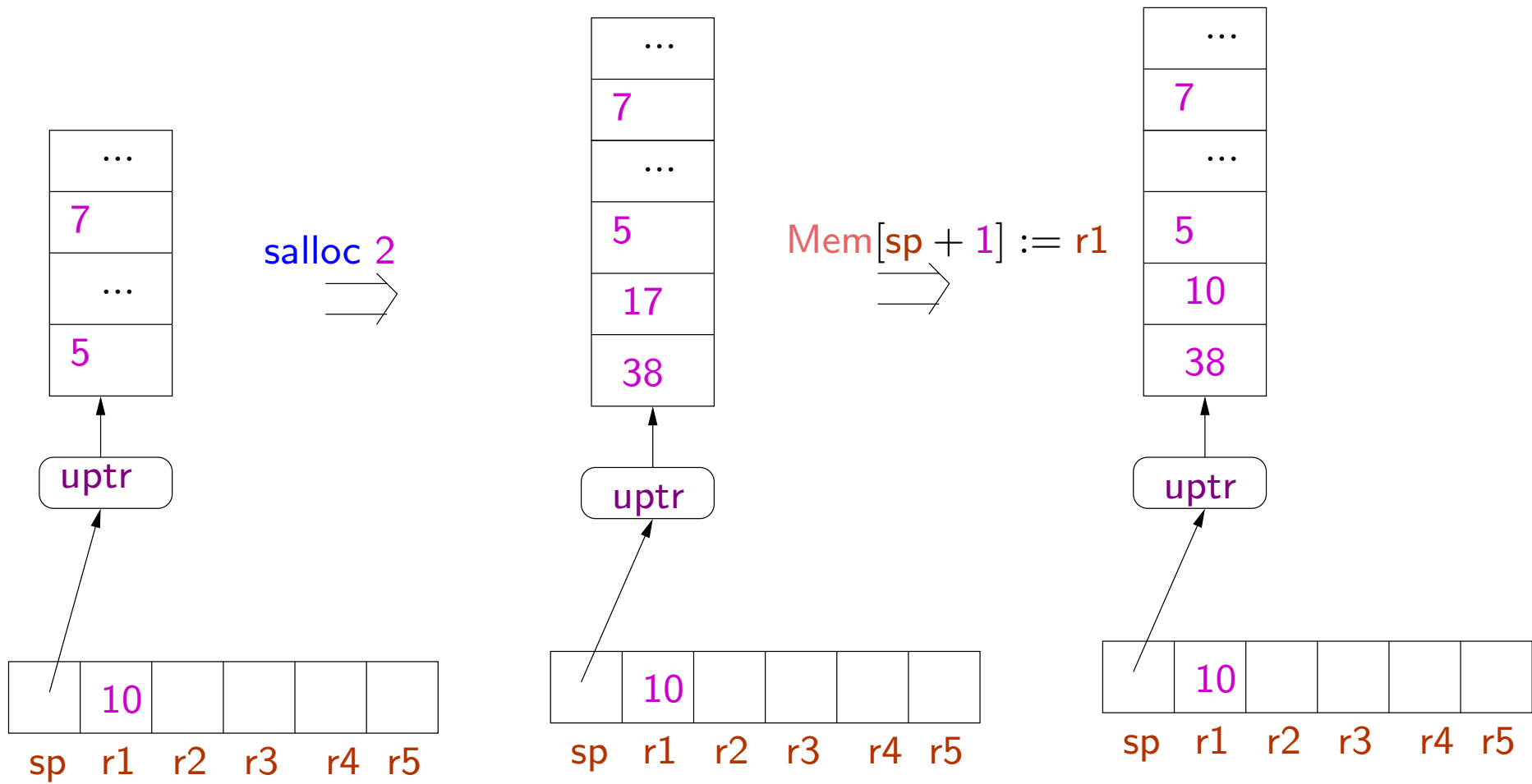
$$\frac{R(\text{sp}) = \text{uptr}\langle \nu_0, \dots, \nu_p \rangle \quad p + n \leq \text{MaxStack}}{(H, R, \text{salloc } n; I) \rightarrow (H, R \oplus \{\text{sp} \mapsto \text{uptr}\langle m_1, \dots, m_n, \nu_0, \dots, \nu_p \rangle\}, I)} \quad (\text{E-Salloc})$$

- The stack is a unique data.
- Instead of allocating a new tuple, we extend the existing stack
- Arbitrary integers (uninitialized values) are added at the top of the stack.
- Stack overflow leads to stuck state.
- We have chosen the stack to grow upward: positive indexing as for other data tuples.

## Deallocating space from the stack

$$\frac{R(\text{sp}) = \text{uptr}\langle \nu'_1, \dots, \nu'_n, \nu_0, \dots, \nu_p \rangle}{(H, R, \text{sfree } n; I) \rightarrow (H, R \oplus \{\text{sp} \mapsto \text{uptr}\langle \nu_0, \dots, \nu_p \rangle\}, I)} \quad (\text{E-Sfree})$$

- Stack underflow leads to a stuck state: the stack should have at least  $n$  elements before the `sfree` instruction.



- No `call/return` instructions in the language.
- These are simulated using the `jump` instruction: e.g. saving/restoring return addresses are done explicitly.
- Allows modifications in `calling conventions` (passing arguments and return address on stack or in registers, tail recursion, ...)
- For this we focus on a more primitive set of type constructors.
- In contrast, the JVM language has notions of procedures and procedure calls hardwired into the language. Any modification (e.g. adding tail recursion) requires modifications in the abstract machine and the type system.

## Translations from high level languages to TAL-0

TAL-0 is expressive enough to implement simple subsets of high level languages.

### Example C Code

```
int fib (int x) {  
    if (x == 0) return 0; else  
    if (x == 1) return 1; else  
    return (fib (n-1) + fib (n-2));  
}
```



We choose the following [calling conventions](#) for our example.

- Caller pushes arguments on the stack.
- Caller puts return address in **r3**.
- Callee pops arguments from the stack.
- Callee returns the result in **r1**.
- Register **r2** is freely available for intermediate computations.

```

fib :  r2 := Mem[sp];           // r2 := x
      if r2 jump ret0;
      r2 := r2 + -1;           // r2 := x - 1
      if r2 jump ret1;
      salloc 2;
      Mem[sp + 1] := r3;       // save old return address
      Mem[sp] := r2;           // push x - 1 on stack
      r3 := cont1;             // new return address
      jump fib                  // r1 := fib(x - 1)

```

```
ret0 :  r1 := 0;    // return value  
       sfree 1;    // pop argument  
       jump r3     // return
```

```
ret1 :  r1 := 1;  
       sfree 1;  
       jump r3
```

```
ret0 :  r1 := 0;    // return value
        sfree 1;   // pop argument
        jump r3    // return
```

```
ret1 :  r1 := 1;
        sfree 1;
        jump r3
```

```
cont1 :  salloc 2;
         Mem[sp + 1] := r1; // save fib(x - 1)
         r2 := Mem[sp + 3]; // r2 := x
         r2 := r2 + -2;     // r2 := x - 2
         Mem[sp] := r2;    // push x - 2 on stack
         r3 := cont2;     // push return address
         jump fib         // r1 = fib(x - 2)
```

```
cont2 : r2 := Mem[sp];      // r2 := fib(x - 1)
        r1 := r1 + r2;      // r1 := fib(x - 2) + fib(x - 1)
        r3 := Mem[sp + 1];  // restore old return address
        sfree 3;
        jump r3
```

## Towards a TAL-1 type system

How to distinguish "good" programs from "bad" programs?

As discussed, we need types

$\text{ptr}(\sigma)$     unique pointer type

$\text{uptr}(\sigma)$     shared pointer type

where  $\sigma$  is an **allocated type**, i.e. type for allocated data.

The instruction  $r1 := \text{malloc } 3$  makes the register  $r1$  to be of type  $\text{uptr}\langle \text{Int}, \text{Int}, \text{Int} \rangle$ .

The instruction  $\text{commit } r2$  transforms the type of register  $r2$  from  $\text{uptr}(\sigma)$  to  $\text{ptr}(\sigma)$ .

Consider the `fib` example again.

Initially `sp` should point to a stack having `int` at the top.

However the rest of the stack could be `arbitrarily large` and have elements of `arbitrary type`.

Consider the `fib` example again.

Initially `sp` should point to a stack having `Int` at the top.

However the rest of the stack could be `arbitrarily large` and have elements of `arbitrary type`.

First idea: use a type similar to `Top`, to represent tuples of "any" type.

Further this should type should also represent tuples of `any length`.

Suppose we choose a type `Top'` for this.



Then `fib` would expect `sp` to have type  $\langle \text{Int}, \text{Top}' \rangle$ , representing a stack with an integer at the top and any number of other things below.

Hence we should expect:

`fib` : `Code`{`sp` : `uptr` $\langle \text{Int}, \text{Top}' \rangle$ , `r1` : `Top`, `r2` : `Top`, `r3` : `Code`( $\Gamma$ )}

What should be  $\Gamma$ ?

At the end of computation, we have `r1` : `Int`, `sp` : `uptr`(`Top'`), and we jump to the label `l` contained in `r3`.

Hence we should expect:

$\Gamma = \{\text{sp} : \text{uptr}(\text{Top}'), \text{r1} : \text{Int}, \text{r2} : \text{Top}, \text{r3} : \text{Top}\}$ .

Then `fib` would expect `sp` to have type  $\langle \text{Int}, \text{Top}' \rangle$ , representing a stack with an integer at the top and any number of other things below.

Hence we should expect:

`fib` : `Code`{`sp` : `uptr` $\langle \text{Int}, \text{Top}' \rangle$ , `r1` : `Top`, `r2` : `Top`, `r3` : `Code`( $\Gamma$ )}.

What should be  $\Gamma$ ?

At the end of computation, we have `r1` : `Int`, `sp` : `uptr`(`Top'`), and we jump to the label `l` contained in `r3`.

Hence we should expect:

$\Gamma = \{\text{sp} : \text{uptr}(\text{Top}'), \text{r1} : \text{Int}, \text{r2} : \text{Top}, \text{r3} : \text{Top}\}$ .

But we are forgetting the relationship between the types of values on the stack at the beginning and at the end!

Solution: use type variables to state such equalities.

Hence with `fib` we will associate the type

$$\forall s \cdot \text{Code}\{\text{sp} : \text{uptr}\langle \text{Int}, s \rangle, r1 : \text{Top}, r2 : \text{Top}, \\ r3 : \text{Code}\{\text{sp} : \text{uptr}(s), r1 : \text{Int}, r2 : \text{Top}, r3 : \text{Top}\}\}$$

where `s` is an `allocated type variable` i.e. representing an arbitrary length of allocated memory.

This expresses the constraint that the code pointed to by `r3` should expect the same type of stack that is below the argument of `fib`.

The universal quantifier helps to distinguish occurrences of the variable `s` elsewhere.

## The TAL-1 type system

$\tau ::=$  operand types

- $\text{Int} \mid \text{Code}(\Gamma)$
- $\mid \text{ptr}(\sigma)$  shared pointer types
- $\mid \text{uptr}(\sigma)$  unique pointer types
- $\mid \forall \rho \cdot \tau$  quantification over allocated types

---

$\sigma ::=$  allocated types

- $\epsilon$  empty tuple type
- $\tau$  one operand
- $\langle \sigma_1, \sigma_2 \rangle$  pair
- $\rho$  allocated type variable

operand types are for operands and allocated data types are for tuples.

As before register file types  $\Gamma$  are of the form  $\{\text{sp} : \tau, \text{r1} : \tau_1, \dots, \text{rk} : \tau_k\}$  where  $\tau, \tau_i$  are operand types.

Similarly heap types  $\Psi$  map labels to operand types.

We consider

$$\langle \langle \sigma_1, \sigma_2 \rangle, \sigma_3 \rangle = \langle \sigma_1, \langle \sigma_2, \sigma_3 \rangle \rangle = \langle \sigma_1, \sigma_2, \sigma_3 \rangle$$

$$\langle \sigma, \epsilon \rangle = \langle \epsilon, \sigma \rangle = \sigma$$

...

# Typing rules

## Typing rules

### Tuples

$$\frac{\forall 1 \leq i \leq n \cdot \Psi, \Gamma \vdash \nu_i : \tau_i}{\Psi, \Gamma \vdash \langle \nu_1, \dots, \nu_n \rangle : \langle \tau_1, \dots, \tau_n \rangle} \text{ (T-Tuple)}$$

## Typing rules

### Tuples

$$\frac{\forall 1 \leq i \leq n \cdot \Psi, \Gamma \vdash \nu_i : \tau_i}{\Psi, \Gamma \vdash \langle \nu_1, \dots, \nu_n \rangle : \langle \tau_1, \dots, \tau_n \rangle} \text{ (T-Tuple)}$$

$$\frac{\Psi, \Gamma \vdash h : \sigma}{\Psi, \Gamma \vdash \text{uptr}(h) : \text{uptr}(\sigma)} \text{ (T-Uptr)}$$



## Typing of instructions

The older rules of TAL-0 remain unmodified, except for the **Mov** instruction, where now copying of unique pointers should be prevented. Hence we have the following new rule.

$$\frac{\Psi, \Gamma \vdash \nu : \tau \quad \tau \neq \text{uptr}(\sigma)}{\Psi \vdash r_d := \nu : \Gamma \rightarrow \Gamma \oplus \{r_d : \tau\}} \text{ (T-Mov1)}$$

## Typing of instructions

The older rules of TAL-0 remain unmodified, except for the **Mov** instruction, where now copying of unique pointers should be prevented. Hence we have the following new rule.

$$\frac{\Psi, \Gamma \vdash \nu : \tau \quad \tau \neq \text{uptr}(\sigma)}{\Psi \vdash r_d := \nu : \Gamma \rightarrow \Gamma \oplus \{r_d : \tau\}} \text{ (T-Mov1)}$$

We add new typing rules for the new instructions.

$$\frac{n \geq 0}{\Psi \vdash r_d := \text{malloc } n : \Gamma \rightarrow \Gamma \oplus \underbrace{\{r_d : \text{uptr}\langle \text{Int}, \dots, \text{Int} \rangle\}}_{n \text{ times}}} \text{ (T-Malloc)}$$

**malloc** creates a unique pointer type.

$$\frac{\Psi, \Gamma \vdash r_d : \text{uptr}(\sigma) \quad r_d \neq \text{sp}}{\Psi \vdash \text{commit } r_d : \Gamma \rightarrow \Gamma \oplus \{r_d : \text{ptr}(\sigma)\}} \text{ (T-Commit)}$$

`commit` creates a shared pointer type.

$r_d$  stores a (label) pointer to the value which has now been moved into the heap.

$$\frac{\Psi, \Gamma \vdash r_s : \text{ptr}\langle \tau_0, \dots, \tau_n, \sigma \rangle}{\Psi \vdash r_d := \text{Mem}[r_s + n] : \Gamma \rightarrow \Gamma \oplus \{r_d : \tau_n\}} \quad (\text{T-Ld-S})$$

$$\frac{\Psi, \Gamma \vdash r_s : \text{ptr}\langle \tau_0, \dots, \tau_n, \sigma \rangle}{\Psi \vdash r_d := \text{Mem}[r_s + \mathbf{n}] : \Gamma \rightarrow \Gamma \oplus \{r_d : \tau_n\}} \quad (\text{T-Ld-S})$$

$$\frac{\Psi, \Gamma \vdash r_s : \text{uptr}\langle \tau_0, \dots, \tau_n, \sigma \rangle}{\Psi \vdash r_d := \text{Mem}[r_s + \mathbf{n}] : \Gamma \rightarrow \Gamma \oplus \{r_d : \tau_n\}} \quad (\text{T-Ld-U})$$

$$\frac{\Psi, \Gamma \vdash r_d : \text{ptr}\langle \tau_0, \dots, \tau_n, \sigma \rangle \quad \Psi, \Gamma \vdash r_s : \tau_n \quad \tau_n \neq \text{uptr}(\sigma')}{\Psi \vdash \text{Mem}[r_d + n] := r_s : \Gamma \rightarrow \Gamma} \text{ (T-St-S)}$$

Updating shared data should not involve a change in type.

$$\frac{\Psi, \Gamma \vdash r_d : \text{ptr}\langle \tau_0, \dots, \tau_n, \sigma \rangle \quad \Psi, \Gamma \vdash r_s : \tau_n \quad \tau_n \neq \text{uptr}(\sigma')}{\Psi \vdash \text{Mem}[r_d + n] := r_s : \Gamma \rightarrow \Gamma} \text{(T-St-S)}$$

Updating shared data should not involve a change in type.

$$\frac{\Psi, \Gamma \vdash r_d : \text{uptr}\langle \tau_0, \dots, \tau_n, \sigma \rangle \quad \Psi, \Gamma \vdash r_s : \tau \quad \tau \neq \text{uptr}(\sigma')}{\Psi \vdash \text{Mem}[r_d + n] := r_s : \Gamma \rightarrow \Gamma \oplus \{r_d : \text{uptr}\langle \tau_0, \dots, \tau_{n-1}, \tau, \sigma \rangle\}} \text{(T-St-U)}$$

$$\frac{\Psi, \Gamma \vdash \text{sp} : \text{uptr}(\sigma) \quad n \geq 0}{\Psi \vdash \text{salloc } n : \Gamma \rightarrow \Gamma \oplus \underbrace{\{\text{sp} : \text{uptr}\langle \text{Int}, \dots, \text{Int}, \sigma \rangle\}}_{n \text{ times}}} \text{(T-Salloc)}$$



$$\frac{\Psi, \Gamma \vdash \text{sp} : \text{uptr}(\sigma) \quad n \geq 0}{\Psi \vdash \text{salloc } n : \Gamma \rightarrow \Gamma \oplus \underbrace{\{\text{sp} : \text{uptr}\langle \text{Int}, \dots, \text{Int}, \sigma \rangle\}}_{n \text{ times}}} \text{ (T-Salloc)}$$

$$\frac{\Psi, \Gamma \vdash \text{sp} : \text{uptr}\langle \tau_1, \dots, \tau_n, \sigma \rangle}{\Psi \vdash \text{sfree } n : \Gamma \rightarrow \Gamma \oplus \{\text{sp} : \text{uptr}(\sigma)\}} \text{ (T-Sfree)}$$

$$\frac{\Psi, \Gamma \vdash \text{sp} : \text{uptr}(\sigma) \quad n \geq 0}{\Psi \vdash \text{salloc } n : \Gamma \rightarrow \Gamma \oplus \underbrace{\{\text{sp} : \text{uptr}\langle \text{Int}, \dots, \text{Int}, \sigma \rangle\}}_{n \text{ times}}} \text{ (T-Salloc)}$$

$$\frac{\Psi, \Gamma \vdash \text{sp} : \text{uptr}\langle \tau_1, \dots, \tau_n, \sigma \rangle}{\Psi \vdash \text{sfree } n : \Gamma \rightarrow \Gamma \oplus \{\text{sp} : \text{uptr}(\sigma)\}} \text{ (T-Sfree)}$$

Stack underflows are ruled out by the type system.

What about stack overflows??

The type system is not powerful enough to keep track of the size of stack.

Hence Code leading to stack overflow will be well-typed, violating safety.

To ensure type safety, we add new evaluation rules in case of stack overflow.

The type system is not powerful enough to keep track of the size of stack.

Hence Code leading to stack overflow will be well-typed, violating safety.

To ensure type safety, we add new evaluation rules in case of stack overflow.

$$\frac{R(\text{sp}) = \text{uptr}\langle \nu_0, \dots, \nu_p \rangle \quad p + n > \text{MaxStack}}{(H, R, \text{salloc } n; I) \rightarrow \text{StackOverflow}} \quad (\text{E-Overflow1})$$

Where **StackOverflow** is a new special machine state.

This is similar to "error" terms in our previous discussion on type safety.

The rules for typing instruction sequences, register files, heaps and machine states are as for TAL-0.

We further require rules for quantifying over allocated type variables, and for generating instances.

The rules for typing instruction sequences, register files, heaps and machine states are as for TAL-0.

We further require rules for quantifying over allocated type variables, and for generating instances.

$$\frac{\Psi \vdash I : \tau}{\Psi \vdash I : \forall \rho \cdot \tau} \text{ (T-Gen)}$$

$\rho$  is an allocated type variable possibly occurring in  $\tau$ .

Type of labels can be instantiated by the following rule.

We replace occurrences of  $\rho$  by any desired type  $\tau'$ .

$$\frac{\Psi, \Gamma \vdash \nu : \forall \rho \cdot \tau}{\Psi, \Gamma \vdash \nu : \tau[\rho \mapsto \tau']} \text{ (T-Inst)}$$

## Example

```
ret0 :  r1 := 0;    // return value
        sfree 1;    // pop argument
        jump r3     // return
```

We would like to assign to this instruction sequence, the type

$\tau = \forall s \cdot \text{Code}\{\Gamma\}$  where

$\Gamma = \{\text{sp} : \text{uptr}\langle \text{Int}, s \rangle, \text{r1}, \text{r2} : \text{Top}, \text{r3} : \text{Code}\{\text{sp} : \text{uptr}(s), \text{r1} : \text{Int}, \text{r2}, \text{r3} : \text{Top}\}\}$

where allocated type variable  $\text{sp}$  represents an arbitrary chunk of memory.

Let  $\Gamma_1 = \Gamma \oplus \{\text{r1} : \text{Int}\}$  and  $\Gamma_2 = \Gamma_1 \oplus \{\text{sp} : \text{uptr}(s)\}$ .

For any heap type  $\Psi$  we have the following typing derivation.

$$\begin{array}{c}
 \vdots \\
 \Psi, \Gamma_2 \vdash r3 : \text{Code}\{\text{sp} : \text{uptr}(s), r1 : \text{Int}, r2, r3 : \text{Top}\} \quad \text{Code}(\Gamma_2) \sqsubseteq \text{Code}\{\dots\} \\
 \hline
 \Psi, \Gamma_2 \vdash r3 : \text{Code}(\Gamma_2) \\
 \hline
 \Psi \vdash \text{jump } r3 : \text{Code}(\Gamma_2)
 \end{array}
 \quad (\text{T-Sub})$$

(T-Jump)



$$\frac{\Psi, \Gamma_2 \vdash r3 : \text{Code}\{\text{sp} : \text{uptr}(s), r1 : \text{Int}, r2, r3 : \text{Top}\} \quad \text{Code}(\Gamma_2) \sqsubseteq \text{Code}\{\dots\}}{\Psi, \Gamma_2 \vdash r3 : \text{Code}(\Gamma_2)} \text{ (T-Sub)}$$

$$\frac{\Psi, \Gamma_2 \vdash r3 : \text{Code}(\Gamma_2)}{\Psi \vdash \text{jump } r3 : \text{Code}(\Gamma_2)} \text{ (T-Jump)}$$

$$\frac{\Psi, \Gamma_1 \vdash \text{sp} : \text{uptr}\langle \text{Int}, s \rangle \quad \Psi \vdash \text{jump } r3 : \text{Code}(\Gamma_2)}{\Psi \vdash \text{sfree } 1 : \Gamma_1 \rightarrow \Gamma_2} \text{ (T-Sfree)}$$

$$\frac{\Psi \vdash \text{sfree } 1 : \Gamma_1 \rightarrow \Gamma_2 \quad \Psi \vdash \text{jump } r3 : \text{Code}(\Gamma_2)}{\Psi \vdash \text{sfree } 1; \text{jump } r3 : \text{Code}(\Gamma_1)} \text{ (T-Seq)}$$

$$\frac{\Psi \vdash r1 := 0 : \Gamma \rightarrow \Gamma_1 \quad \Psi \vdash \text{sfree } 1; \text{jump } r3 : \text{Code}(\Gamma_1)}{\Psi \vdash r1 := 0; \text{sfree } 1; \text{jump } r3 : \text{Code}(\Gamma)} \text{ (T-Seq)}$$

$$\frac{\Psi \vdash r1 := 0; \text{sfree } 1; \text{jump } r3 : \text{Code}(\Gamma)}{\Psi \vdash r1 := 0; \text{sfree } 1; \text{jump } r3 : \forall s \cdot \text{Code}(\Gamma)} \text{ (T-Gen)}$$